also respectfully submit that the rejection based on Nishi in view of Apperley is an improper rejection because the Apperley patent is unavailable as a reference.

More specifically, a careful review of the Apperley reference shows that its availability as a reference against the present application is based on either the effective date of the Apperley patent under 35 USC §102(e) or the PCT Publication date. In particular, the 102(e) date is set forth on the face of the patent as April 2, 1993. This effective 102(e) filing date is subsequent to the PCT publication date of September 3, 1992. Both of these dates are actually prior to the effective U.S. filing date of the present application of June 22, 1993. However, both the 102(e) date and the PCT publication date for the Apperley patent are subsequent to the applicants' Japanese priority date under 35 USC §119, of June 22, 1992 based on the Japanese priority document 4-163074.

As noted in the Appeal Brief, the feature found in each of the independent claims 1 and 16 of first and second erase commands to different nonvolatile memories is an important feature of the present claimed invention. For the Examiner's convenience, a copy of a machine translation of the detailed description of the Japanese Priority Document 4-163074 is provided herewith (noting that a certified copy of this Japanese Priority Document was originally filed in the great grandparent application Serial No. 08/079,550 (now USP 5,530,828). This detailed description provided herewith is taken from one of the Japanese divisional applications, published as JP 2000-148583, of the original Japanese Priority Document 4-163074, and, on information and belief, is believed to correspond to the actual detailed description of the parent priority document 4-163074 for the divisional JP 2000-148583. Regarding this, the undersigned attorney is in the process of

seeking to obtain a sworn translation of the original priority document 4-163074 to provide to the Examiner for review in this matter.

Referring to the attached detailed description, it can be seen that paragraph [0019] on page 4 essentially corresponds to the description found in the paragraph bridging pages 16 and 17 of the present application. The machine translation describes the erase operation for data in the flash memories in terms of the word "elimination" but it is clear from the description in paragraph [0019] that support exists in the priority document for the plural erase operations described in the last two paragraphs of each of claims 1 and 16 of the present application. Therefore, it is respectfully submitted that the Japanese priority document 4-163074 for the present application on appeal overcomes the use of Apperley as a reference. Once Apperley is unavailable as a reference, the 35 USC §103 rejection set forth in the Final Office Action no longer stands. Therefore, reconsideration and removal of this rejection, and allowance of the present application, is respectfully requested.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 566.32253CC8), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
Gregory E. Montone
Reg. No. 28,141

GEM/dks
Attachment: machine translation of JP 2000-148583

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] It is related with this invention writing in data about the semiconductor memory which used the flash memory succeeding the RAM disk equipment especially using a flash memory etc.
[0002]
[Description of the Prior Art] The timing wave [flash memory / which performs writing and elimination by the command control method concerning the conventional technique] of data writing is shown in drawing 8 . It is the supply voltage of a flash memory and regular +5V are impressed by the inside Vcc of drawing. Vpp is a write-in power source, and when writing in data to a flash memory, it impresses potential higher than supply voltage Vcc. The address specifies the write-in field of the data of a flash memory per cutting tool. OE is an output enable signal, in case it reads data from a flash memory, it sets to Low, and it is made into High at the time of others. CE is a chip enable signal, and when performing the read-out writing of a command or data to a flash memory, it is taken as Low. Moreover, CE of this flash memory serves also as the write enable signal, Vpp is high potential, and when OE is High, data are written in in the standup of OE. I/O7 and I/O0 - I/O6 are the data lines. Then, the actuation when writing 1 byte of data in a flash memory is shown. First, the command on the data line is written in a flash memory to the timing of the standup of CE. This command is a light setup command which tells a flash memory about initiation of the writing of 1-word data. The data on the data line are written in a flash memory to the timing of the standup of CE after the writing of this command. The Low period of CE at the time of the writing of this command and data is a minimum of 50 nanoseconds. However, in fact, inside a flash memory, the following data cannot be written in until the writing to a memory chip just started and the writing in the interior is completed. The time amount for dozens of microseconds is required, it is, and most time amount is taken to complete the writing inside a flash memory here as compared with the time amount of the writing of a command and 1-word data. And there is status polling as a means to investigate that the writing inside a flash plate memory chip was completed, through this time amount for dozens of microseconds. This sets CE and OE to Low, reads the status from I/O7, and judges termination of writing inside a memory chip.
[0003]
[Problem(s) to be Solved by the Invention] The above-mentioned technique requires most time amount, when writing in two or more words data continuously. The writing of a command and 1-word data is about hundreds of nanoseconds from dozens of nanoseconds. However, after writing in 1-word data, by the time the writing inside a flash plate memory chip is completed, the time amount for several microseconds to dozens of microseconds is required, and a flash memory cannot be accessed in the meantime. Therefore, the total time amount for writing in 1-word data reads, and it is quite late as compared with time amount. Moreover, when writing in two or more words data continuously, it writes in in proportion to the numbers of words to write in, and time amount increases. For example, when RAM disk equipment is built using a flash memory, dozens kilo word or the data beyond it is continuously written in from number kilo word. If it does so, since it will write in in proportion to the

data written in and time amount will increase, a transfer of writing becomes slow as the whole system.
[0004] The purpose of this invention is offering the semiconductor memory which shortened the write-in time amount of data.
[0005]
[Means for Solving the Problem] It carries out having the control section this invention carries two or more flash memories, and write in to as another flash memory as the above-mentioned flash memory to which writing will be performed by the time the above-mentioned flash memory by which write-in directions were sent to the above-mentioned flash memory in delivery and write-in directions becomes receivable [the following write-in directions] in the semiconductor memory which performs a data storage to the above-mentioned flash memory in order to solve the above-mentioned problem, and send directions.
[0006] More concretely, this invention can make two or more bits 1 word, can read them to a word unit, and can be written in. In the equipment which carries two or more eliminable flash EEPROMs electrically per a chip unit or two or more words, and writes in data succeeding the above-mentioned flash memory The above-mentioned flash memory to which it wrote in said flash memory of the arbitration in which 1-word data were carried by the above-mentioned write-in equipment, and writing was performed the data which are the following 1 word between fixed time amount whose writing is attained It is characterized by writing 1-word data in a flash memory other than said flash memory to which the writing carried in said equipment is performed.
[0007]
[Function] Two or more flash memories are carried, and in the semiconductor memory which performs a data storage to the above-mentioned flash memory, a control section is written in a flash memory other than the above-mentioned flash memory to which writing will be performed by the time the above-mentioned flash memory by which write-in directions were sent to the above-mentioned flash memory in delivery and write-in directions becomes receivable [the following write-in directions], and sends directions.
[0008]
[Example] In the writing of continuous data, it controls by this example not to write in the same flash memory continuously, but to write in other flash memories. After writing 1-word data in a flash memory before writing in the following data, there is the latency time for several microseconds to dozens of microseconds. Therefore, writing 1-word data in other flash memories, when it writes in continuously and there are data is continued succeeding between this latency time. And if it passes over the latency time of the flash memory written in first, status polling will be performed from the first flash memory, and the 1-word data as follows will be written in. Thus, the writing to other flash memories is performed between the latency times of a flash memory.
[0009] When a flash memory is used for the application which writes in the data with which plurality continued, according to this example, the writing of the low speed of a flash memory can be accelerated in total of equipment. That is, when a flash memory is used for RAM disk equipment, the data with which plurality continued are written in. However, in the writing of continuous data, since it is late as compared with read-out, a total transfer rate falls [the writing to a flash memory]. However, even if the writing of a flash memory is a low speed according to this example, improvement in the speed of the writing of the whole equipment is realizable.
[0010] Drawing is used for below and one example of this invention is explained to it at a detail.
Drawing 1 is the block diagram of the RAM disk equipment which used the flash memory. One in drawing is standard buses, such as a personal computer, and performs transfer of the command from a system, or data through this bus. If said bus, in addition to this, has the agreement of a protocol with the system which needs auxiliary storage units, such as a SCSI interface and a local bus of a system, there will be especially no limitation. 4 is two or more flash memories. 5 is the light buffer memory for holding the data transmitted from the standard bus 1 temporarily. Since writing is slow as compared with read-out, a flash memory holds the write-in data transmitted from a standard bus 1 temporarily, and opens the right of a bus early to a system side. The light buffer memory 5 consists of static RAMs all

over drawing. However, not only regardless of a static RAM but regardless of volatility and a non-volatile, what is necessary is just the storage element which can be written in from a flash memory 4 at a high speed. Moreover, a part of data storage area not only in the inside of RAM disk equipment but a system side may be used. The light buffer memory 5 is the 512-byte unit which is the sector capacity of a standard disk, and has the capacity of two or more sectors. 2 is a processor. This processor 2 performs transfer and analysis of control of the writing of the data from the light buffer memory 5 to a flash memory 4, the command from a standard bus, or the status. 11 is static RAM (SRAM) which has memorized the translation table (a processor 2 creates a translation table about the logical sector number accessed by beginning) which changes the logical sector number which is a sector number which a system manages into the physical sector number which is a sector number of the field to a flash memory to write in. 31 is an address control section which generates the physical address which is an actual address of a flash memory 4 or the light buffer memory 5, and is controlled by the processor 2. 6 is a Vpp generating circuit which generates Vpp which is the write-in power source of a flash memory, and has power-source generating controlled by the processor 2. 71 is the memory address bus of a flash memory 4 or the light buffer memory 5, and is outputted from the address control section 31. 72 is a data bus.

[0011] In the RAM disk equipment of the configuration of drawing 1 , the write-in actuation which a processor 2 controls is shown in the flow chart of drawing 2 . When it judges whether it is the demand of writing from a standard bus 1 and (21) and a demand come, a processor 2 is written in to the Vpp generating circuit 6, and starts generating of a power source Vpp (22). And a processor 2 changes the logical sector number which is a sector number which was passed from the standard bus 1, and which a system manages into the physical sector number which is a sector number of the field to a flash memory to write in (23). Under the present circumstances, a physical sector number is determined so that the flash memory which writes in the data of two or more sectors transmitted from a standard bus 1 per sector, respectively may become another chip. for example, the data of 1 sector to which the data of 1 sector transmitted first are transmitted by the chip 0 of a flash memory at a degree -- the chip 1 of a flash memory -- ** -- it assigns the condition to say per sector. It holds on the write-in managed table in which drawing 3 shows this determined physical sector number. This write-in managed table exists in the address control section 31. By drawing 3 , the data for 3 sectors transmitted from a standard bus 1 are held from the block 1 of the light buffer memory 5 to block 3, and writing the data of 1 sector of each block in the sector 3 of the chip 0 of a flash memory 4, the sector 2 of a chip 1, and the sector 7 of a chip 2, respectively is shown.

[0012] And if a setup of a write-in managed table is completed, they will be received from the block 1 of the light buffer memory 5 to three fields of block 3 as a write-in managed table specifies the data of 3 sectors transmitted from a standard bus 1. The access privilege of a standard bus 1 is opened wide, and it enables it to process the writing to a flash memory 4 only within RAM disk equipment by that cause (24).

[0013] And the data received to the light buffer memory 5 are written in the flash memory 4. First, the physical address of the light buffer memory 5 or a flash memory 4 is outputted to the memory address bus 71 by a processor's 2 writing in and choosing the table number 0 of a managed table. Therefore, 1-word data are read from the block 1 of the light buffer memory 5, and (26) and the 1-word data which wrote the light command in the chip 0 of a flash memory 4, and were read from (27) and the light buffer memory 5 are written in the chip 0 of a flash memory 4 (28). Now, although the writing of the data in the interior is started, as for a chip 0, R/W of data cannot do the chip 0 of a flash memory 4 until the writing in the interior is completed. It judges whether there are any data written in the following chip, and the writing to memory chip another in the meantime is performed at (29) and a certain time. As stated at the time of conversion to a physical sector, it is assigned to another chip for every sector at the time of the writing of a consecutive sector. A processor 2 writes in and the 1-word data which specified the table number 1 of a managed table and were read from the block 2 of (25) and the light buffer memory 5 are written in the chip 1 of a flash memory 4 (26, 27, 28). Continuously, the table number 2 is specified and the 1-word data read from the block 3 of the light buffer memory 5 are written in the chip

2 of a flash memory 4 (26, 27, 28).

[0014] the chip 0 of a flash memory 4, a chip 1, and a chip 2 -- if it is alike, respectively and finishes writing 1-word data, it will be checked whether performed status polling of the chip 0 of the flash memory 4 written in (29) and the beginning, and the writing inside (33) and the chip of a flash memory 4 has been completed. The status of the chip 0 of a flash memory 4 is read by a processor's 2 writing in and specifying the table number 0 of a managed table like writing also at this time. Status polling is repeated if writing is not completed inside the chip 0 of a flash memory 4 here. If writing is completed, the counter value of the table 0 of a write-in managed table will be incremented (34). Similarly it judges whether the following table is shown in a write-in managed table, and the table number 1 is specified at (35) and a certain time, and they perform status polling of the chip 1 which wrote data in the degree of the chip 0 of a flash memory 4. And if the writing inside the chip 1 of a flash memory 4 is completed, status polling of the chip 2 of the flash memory 4 which wrote data in the degree will be performed (33). If all the chips of the flash memory 4 which wrote in have ended the writing in the interior, they will return to the beginning of a write-in sequence.

[0015] It judges whether the counter amounts to 512 bytes, and if it has reached, it means that the writing of all the data from buffer memory 5 to a flash memory 4 was completed here. When a counter is still 512 bytes or less, it repeats until 512 bytes of writing is continuously completed by the aforementioned write-in method. And if the writing of all the data from the light buffer memory 5 to a flash memory 4 is completed, a processor 2 will be written in to the Vpp generating circuit 6, and will stop generating of a power source Vpp (37).

[0016] Also in said example, the writing to a flash memory can perform the data of 3 sectors by the write-in time amount of about 1 sector so that clearly. Although this example showed the example of 3 sectors writing, this with the same more nearly said of the writing of the data of many sectors than 3 sector is clear.

[0017] Moreover, although said example assigned the flash memory written in per sector to another chip, it also has the approach of dividing into the block of the plurality in a sector 512 bytes. Writing is assigned to a flash memory which is different in the divided block unit. For example, it divides into 16 blocks by making 512 bytes into a 32-byte unit. And 16 blocks is written in the chip with which flash memories differ, respectively from 1 block. Although this considered as the 32-byte unit, it is good per cutting tools of arbitration, such as 16 bytes and 64 etc. bytes.

[0018] Moreover, said example showed the flash memory with the latency time fixed to the writing of the 1-word data as follows, after writing in a light command and 1-word data. However, after writing in the flash memory which can do page writing, i.e., a page light command The flash memory which has the fixed latency time after being able to write two or more words data in continuation and writing in the data which are two or more words before the writing to a memory chip is completed inside a flash memory Like said example, after writing in data per page, the data to flash plate memory chip with the another flash plate memory chip which wrote data in the time amount to status polling are written in.

[0019] Moreover, it can say that it is the same not only about the writing of the data to a flash memory 4 but elimination. A flash memory 4 eliminates a chip unit or two or more words in the block unit made into one unit. The elimination approach is writing an elimination command in assignment of the address which shows the block eliminated to a flash memory 4, and coincidence, and starts elimination processing in the flash memory 4 interior. And it becomes the latency time of fixed time amount until elimination in the flash memory 4 interior is completed. Access except status polling cannot be performed in the meantime to the flash memory 4 which is performing elimination processing. And if termination of elimination inside is checked by status polling after fixed time amount passes, it will move to elimination of the following flash memory. Improvement in the speed of elimination with the whole RAM disk equipment is realized by writing an elimination command in a flash memory other than the flash memory which is performing elimination, and eliminating two or more flash memories to coincidence between this fixed time amount.

[0020] In the RAM disk equipment of the configuration of drawing 1 , the elimination actuation which a processor 2 controls is shown in the flow chart of drawing 4 . Since there is the need of writing in also at

the time of elimination of a flash memory 4, and impressing a power source Vpp, a processor 2 is written in to the Vpp generating circuit 6, and starts generating of a power source Vpp (41). And a processor 2 sets the physical sector number of the flash memory 4 to eliminate as the write-in managed table of drawing 3 (42). At this time, it sets up so that the field to eliminate may become another memory chip. This example describes the case where the elimination unit of a flash memory 4 is 1 sector. After setting up the sector eliminated on a write-in managed table, an elimination command is written in each chip of the flash memory 4 of (43) and a table put and shown, updating assignment of a write-in managed table (44). It is checked whether performed the memory chip which updated table assignment and wrote the elimination command in (46) and the beginning when or or a judgment was made and all the writing of (45) and an elimination command was completed to status polling to which an elimination [degree] field is, and elimination processing in (47) and the flash memory 4 interior has been completed. And if the existence of table [degree] assignment is judged and (48) and elimination processing of all flash memories are completed, a processor 2 will be written in to the Vpp generating circuit 6, and will stop generating of a power source Vpp (49).

[0021] The above-mentioned example described the flash memory which performs elimination in 1 sector unit. However, an elimination unit changes with flash memories. Therefore, it writes in by the difference in the elimination unit of a flash memory, and the setting approach of a managed table is changed. In elimination of a flash memory in a chip unit, it is good at a setup of only the column of the chip number of the flash memory of a write-in managed table. Moreover, in the case of the flash memory which eliminates per two or more words, it becomes the set of two columns of the chip number and sector number of the flash memory of a write-in managed table. However, even if it is the flash memory which eliminates per two or more words, it is not necessarily elimination in 1 sector unit. When a flash memory eliminates the capacity which is two or more sectors as 1 block, it becomes elimination of two or more sectors by setting up the column of the sector number of the flash memory of a write-in managed table.

[0022] In said example, when the write-in power sources Vpp, such as the time of writing or elimination, are required, it writes in all the flash memories 4, and the power source Vpp is impressed. However, there is also a method of impressing the write-in power source Vpp only to the flash memory which writes in. The block diagram of the RAM disk equipment which is the example is shown in drawing 5 . It is the switch section which writes in a flash memory 4 from the Vpp generating circuit 6, and turns impression of a power source Vpp on and off, and 61 in drawing is controlled by the processor 2, and selection of the output of two or more write-in power sources Vpp is possible for it. Others are the same configurations as drawing 1 . When the demand of writing comes from a standard bus 1, a processor 2 is written in to the Vpp generating circuit 6, and starts generating of a power source Vpp. Then, a logical sector number is changed into a physical sector number, and a physical sector number is held on the write-in managed table of drawing 2 . At this time, the write-in power source Vpp to the plurality or one flash memory 4 which writes in is impressed by assignment of the Vpp switch section 61, respectively. The impression of carry [not only the time of writing but when the flash memories 4, such as elimination, write in and you need a power source Vpp] by assignment of the Vpp switch section 61 of this write-in power source Vpp is clear.

[0023] Moreover, said example described the flash memory which needs the write-in power source Vpp of a different electrical-potential-difference value from supply voltage at the time of writing or elimination. However, the block diagram of the RAM disk equipment which carried the flash memory of a single power supply and the flash memory in which it writes in short and a power source Vpp does not have the need is shown in drawing 6 . Although the configuration is the same as drawing 1 , there is no need of carrying the Vpp generating circuit 6. Moreover, it is clear that write in with the write-in flow chart of drawing 2 and the flow chart of elimination of drawing 4 , and on-off processing of a power source becomes that there is nothing in the need.

[0024] Moreover, in said example, the chip of the flash memory to write in is chosen by the chip enable signal CE. However, there is the approach of controlling selection of the flash memory written in not by the chip enable signal CE but by the write enable signal WE. The block diagram of the RAM disk

measure at that time is shown in drawing 7 . 32 in drawing is WE selection section which gives the write enable signal WE to the flash memory 4 which writes in alternatively to a flash memory 4. Others are the same configurations as drawing 1 . WE selection section 32 confirms a write enable signal only to the flash memory which writing generated. Control of the writing which a processor 2 performs becomes the same as the actuation which the flow chart of drawing 2 shows.

[0025] Moreover, there is a thing without the write enable signal WE in a flash memory 4. In writing data in this flash memory, it controls writing by control of the chip enable signal CE and the write-in power source Vpp. Even if it is such a flash memory, improvement in the speed of writing or elimination can be attained using this invention.

[0026] Even if writing uses a low speed flash memory for an auxiliary storage unit with a lot of write-in data etc. as compared with read-out according to this invention so that clearly from the above explanation, there is effectiveness that the writing in the whole equipment can be performed at a high speed. Effectiveness is large when there is writing of a lot of data which continued especially. Moreover, it is eliminable at a high speed also about elimination of two or more field coincidence.

[0027]

[Effect of the Invention] Since this invention is constituted as mentioned above, it can offer the semiconductor memory which shortened the write-in time amount of data.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The bus interface which is connected to a system bus and receives the command and sector data of a standard disk from this system bus, Two or more non-volatile semi-conductor memory chips which memorize said sector data, It connects with said two or more non-volatile semi-conductor memory chips. Said sector data The buffer memory held as write-in data which should be written in said two or more non-volatile memory chips transmitted through said bus interface from the system side, The semiconductor memory characterized by having said bus interface, said two or more non-volatile semi-conductor memory chips, and the control section connected with said buffer memory.

[Translation done.]